WS6264 8K-Word By 8 Bit

■ DESCRIPTION

The WS6264 is a high performance; high speed and super low power CMOS Static Random Access Memory organized as 8,192 words by 8bits and operates from a wide range of 2.2 to 5.5V supply voltage. Advanced CMOS technology and circuit techniques provide both high speed, super low power features and maximum access time of 55/70ns in 3.0V operation. Easy memory expansion is provided by an active LOW chip enable (/CE) and active LOW output enable (/OE).

The WS6264 has an automatic power down feature, reducing the power consumption significantly when chip is deselected. The WS626 is available in JEDEC standard 28-pin TSOP I (8x13.4 mm), SOP (330 mil) and PDIP (600 mil) packages.

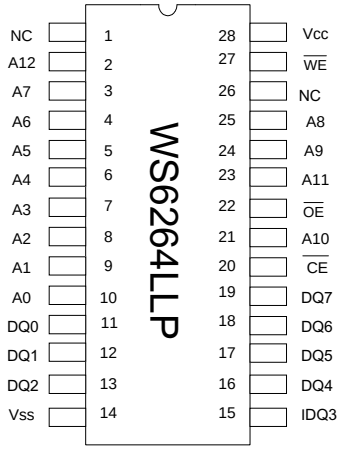
■ FEATURES

- Wide operation voltage : 2.2 ~ 5.5V
- Ultra low power consumption: 2.5mA@1MHz (Max.) , Vcc=5.0V.
  0.2 uA (Typ.) CMOS standby current
- High speed access time: 55~70ns.
- Automatic power down when chip is deselected.
- Three state outputs and TTL compatible.
- Data retention supply voltage as low as 1.5V.
- Easy expansion with /CE and /OE options.

■ PRODUCT FAMILY

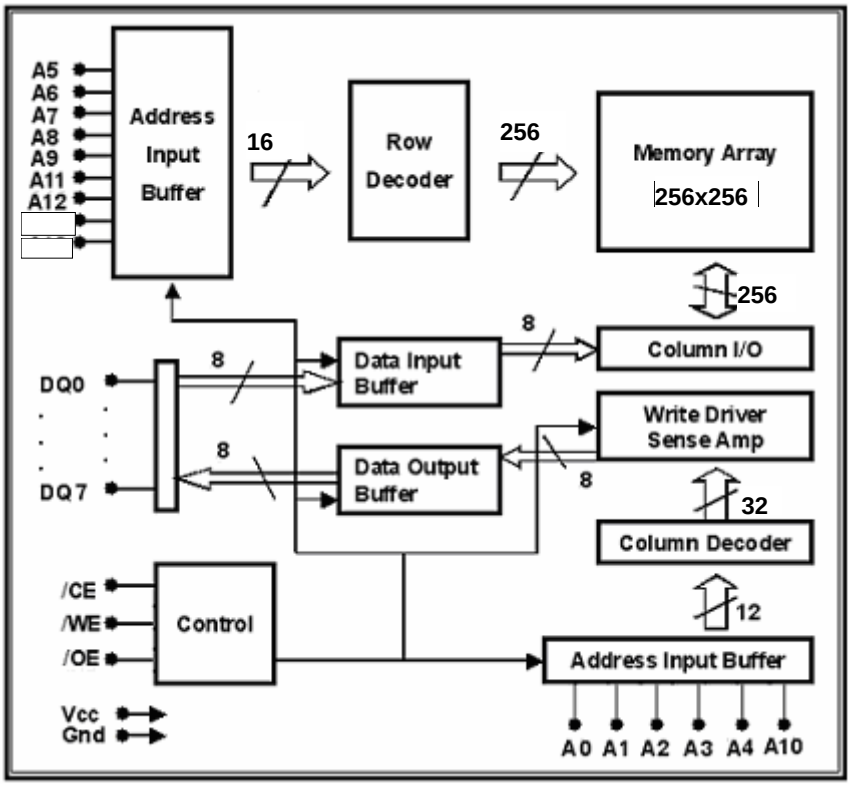
Part No.	Operating Temp.	Vcc Range	Speed (ns)	Standby Current (Typ.) I_{CCSB1}	Package Type
WS6264LLFP	0~70°C	2.2~5.5V	55/70	0.20uA (Vcc = 5.0V)	28 SOP
WS6264LLT					28 TSOP I
WS6264LLP					28 PDIP
WS6264LLFPI	-40~85°C		55/70	0.30uA (Vcc= 3.0V)	28 SOP
WS6264LLTI					28 TSOP I
WS6264LLPI					28 PDIP

■ PIN CONFIGURATIONS



SOP/PDIP

■ BLOCK DIAGRAM



■ PIN DESCRIPTIONS

Name	Type	Function
A0 – A12	Input	Address inputs for selecting one of the 8,192 x 8 bit words in the RAM
/CE	Input	/CE is active LOW. Chip enable must be active when data read from or write to the device. If chip enable is not active, the device is deselected and not in a standby power down mode. The DQ pins will be in high impedance state when the device is deselected.
/WE	Input	The Write enable input is active LOW. It controls read and write operations. With the chip selected, when /WE is HIGH and /OE is LOW, output data will be present on the DQ pins, when /WE is LOW, the data present on the DQ pins will be written into the selected memory location.
/OE	Input	The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when /OE is inactive.
DQ0~DQ7	I/O	These 8 bi-directional ports are used to read data from or write data into the RAM.
Vcc	Power	Power Supply
Gnd	Power	Ground

■ TRUTH TABLE

Mode	/WE	/CE	/OE	I/O state	Vcc Current
Not Selected	X	H	X	High Z	I_{SB},I_{SB1}
Output Disabled	H	L	H	High Z	I_{CC}
Read	H	L	L	D_{OUT}	I_{CC}
Write	L	L	X	D_{IN}	I_{CC}

■ ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Rating	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to Vcc+0.5	V
T_{BIAS}	Temperature Under Bias	-40 to +125	^{O}C
T_{STG}	Storage Temperature	-60 to +150	^{O}C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

■ OPERATING RANGE

Range	Ambient Temperature	Vcc
Commercial	0~70^{o}C	2.2 ~ 5.5V
Industrial	-40~85^{o}C	2.2 ~ 5.5V

■ CAPACITANCE(1)(TA=25℃,f=1.0MHz)

Symbol	Parameter	Conduction	MAX.	Unit
C_{IN}	Input Capacitance	VIN=0V	6	pF
C_{DQ}	Input/Output Capacitance	VDI/O=0V	8	pF

1. This parameter is guaranteed, and not 100% tested.

■ DC ELECTRICAL CHARACTERISTICS (TA =0 to + 70°C)

Name	Parameter	Test Condition	MIN	TYP(1)	MAX	Unit
V_{IL}	Guaranteed Input Low Voltage (2)	Vcc=1.8V	-0.5		0.8	V
V_{IH}	Guaranteed Input High Voltage (2)	Vcc=5.6V	2.0		Vcc+0.2	V
I_{IL}	Input Leakage Current	V_{CC}=MAX, V_{IN}=0 to V_{CC}			1	uA
I_{OL}	Output Leakage Current	V_{CC}=MAX, /CE=V_{IN}, or /OE=V_{IN} , V_{IO}=0V to V_{CC}			1	uA
V_{OL}	Output Low Voltage	V_{CC}=MAX, I_{OL} = 1mA			0.4	V
V_{OH}	Output High Voltage	V_{CC}=MIN, I_{OH} = -0.5mA	1.6			V
I_{CC}	Operating Power Supply Current	/CE=V_{IL}, I_{DQ}=0mA, F=F_{MAX} =1/ t_{RC}			25	mA
I_{CCSB}	TTL Standby Supply	/CE=V_{IH}, I_{DQ}=0mA,			1	mA
I_{CCSB1}	CMOS Standby Current	/CE≧V_{CC}-0.2V, V_{IN}≧ V_{CC}-0.2V or V_{IN}≦0.2V, Vcc=5V		0.2	2	uA

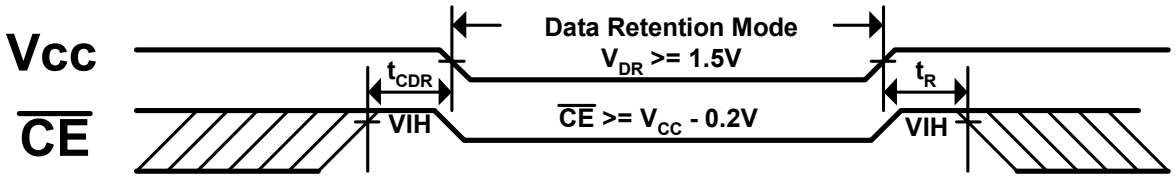
1. Typical characteristics are at TA = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester notice are included.

■ DATA RETENTION CHARACTERISTICS (TA = 0 to + 70°C)

Name	Parameter	Test Condition	MIN	TYP(1)	MAX	Unit
V_{DR}	V_{CC} for Data Retention	/CE ≧ V_{CC}-0.2V, V_{IN} ≧ V_{CC}-0.2V or V_{IN}≦0.2V	1.5			V
I_{CCDR}	Data Retention Current	/CE≧V_{CC}-0.2V, V_{IN}≧ V_{CC}-0.2V or V_{IN}≦0.2V		0.1	0.8	uA
T_{CDR}	Chip Deselect to Data Retention Time	Refer to Retention Waveform	0			ns
t_R	Operation Recovery Time		t_{RC} (2)			ns

1. TA = 25°C.
2. t_{RC}= Read Cycle Time.

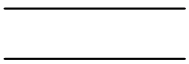
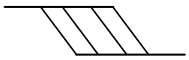
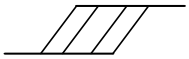
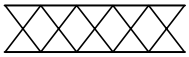
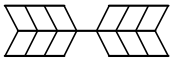
■ LOW Vcc DATA RETENTION WAVEFORM (/CE Controlled)



■ AC TEST CONDITIONS

Input Pulse Levels	Vcc/0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Level	0.5Vcc

■ KEY TO SWITCHING WAVEFORMS

WAVEFORMS	INPUTS	OUTPUTS
	MUST BE STEADY	MUST BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGE FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGE STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE OFF STATE

■ AC TEST LOADS AND WAVEFORMS

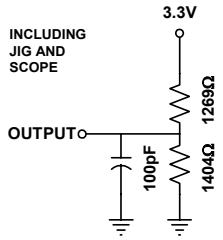


FIGURE 1A

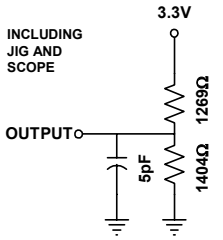
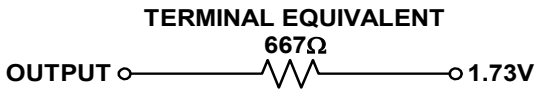


FIGURE 1B



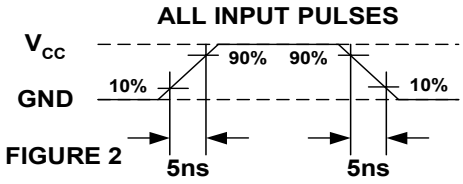


FIGURE 2

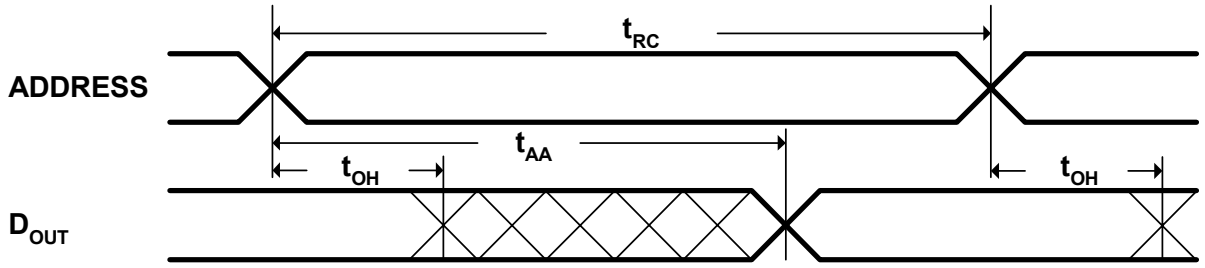
■ AC ELECTRICAL CHARACTERISTICS (TA = 0 to + 70°C, Vcc = 3.0V)

< READ CYCLE >

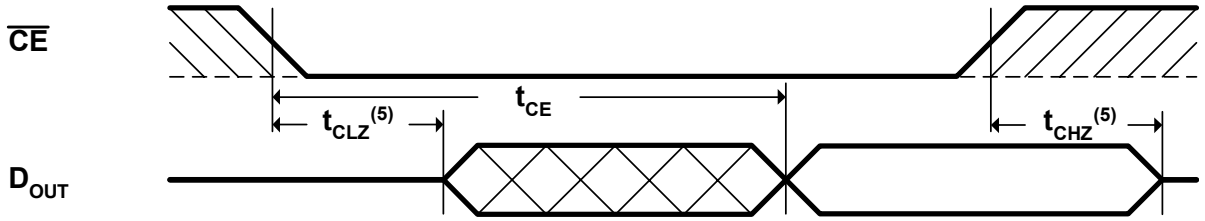
JEDEC Name	Symbol	Description	-55		-70		Unit
			MIN	MAX	MIN	MAX	
t_{AVAX}	t_{RC}	Read Cycle Time	55		70		ns
t_{AVQV}	t_{AA}	Address Access Time		55		70	ns
t_{ELQV}	t_{CE}	Chip Select Access Time		55		70	ns
t_{GLQV}	t_{OE}	Output Enable to Output Valid		30		50	ns
t_{ELQX}	t_{CLZ}	Chip Select to Output Low Z	10		10		ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	5		5		ns
t_{EHQZ}	t_{CHZ}	Chip Deselect to Output in High Z	0	35	0	35	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	0	30	0	30	ns
t_{AXOX}	t_{OH}	Address Change to Out Disable	10		10		ns

■ SWITCHING WAVEFORMS (READ CYCLE)

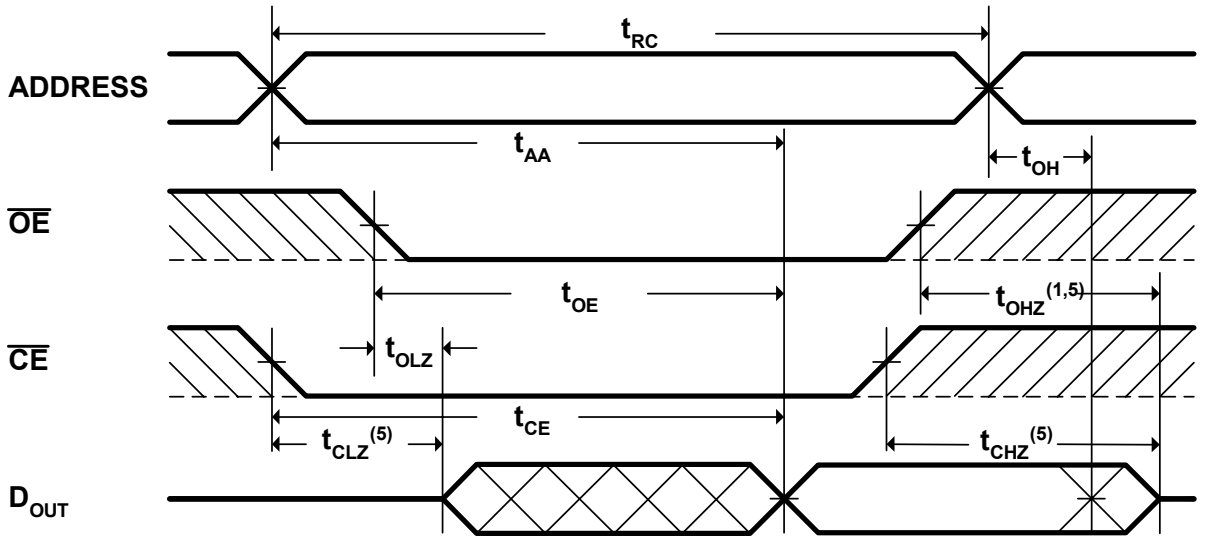
READ CYCLE1 (1,2,4)



READ CYCLE2 (1,3,4)



READ CYCLE3 (1,4)



NOTES:

1. /WE is high in read Cycle.
2. Device is continuously selected when /CE = $V_{IL.}$
3. Address valid prior to or coincident with CE transition low.
4. /OE = VIL.
5. Transition is measured ±500mV from steady state with C_L = 5pF as shown in Figure 1B. The parameter is guaranteed but not 100% tested.

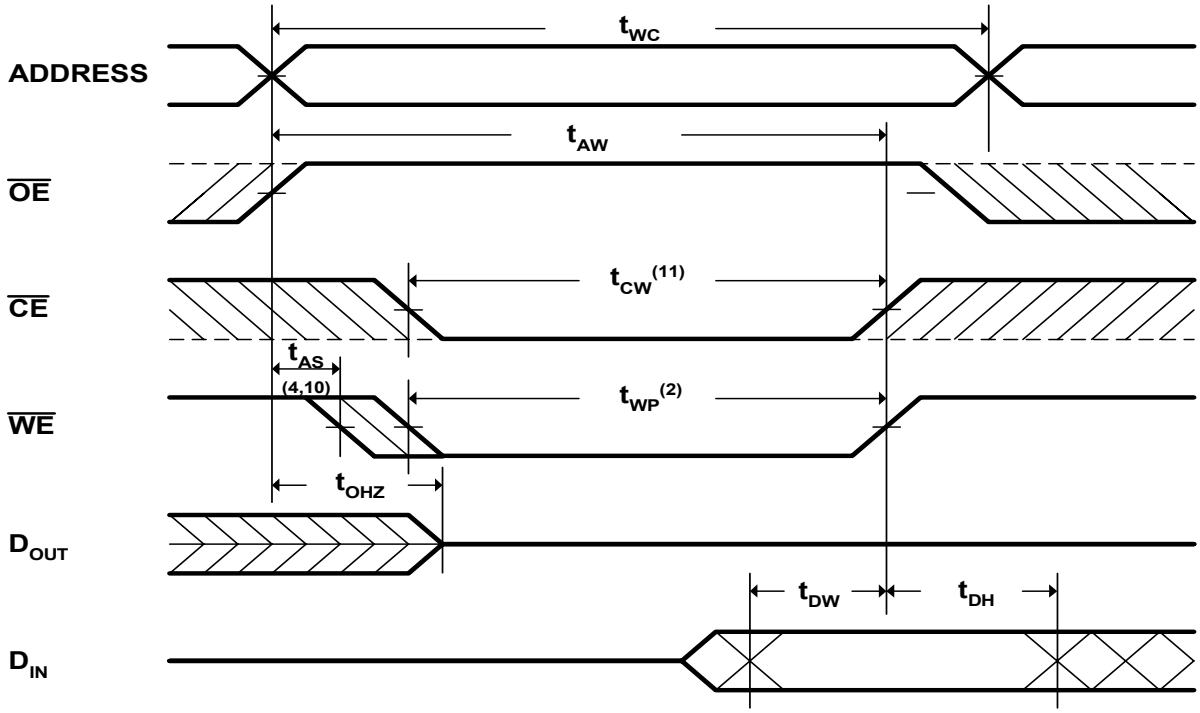
■ AC ELECTRICAL CHARACTERISTICS (TA = 0 to + 70°C , Vcc = 3.0V)

< WRITE CYCLE >

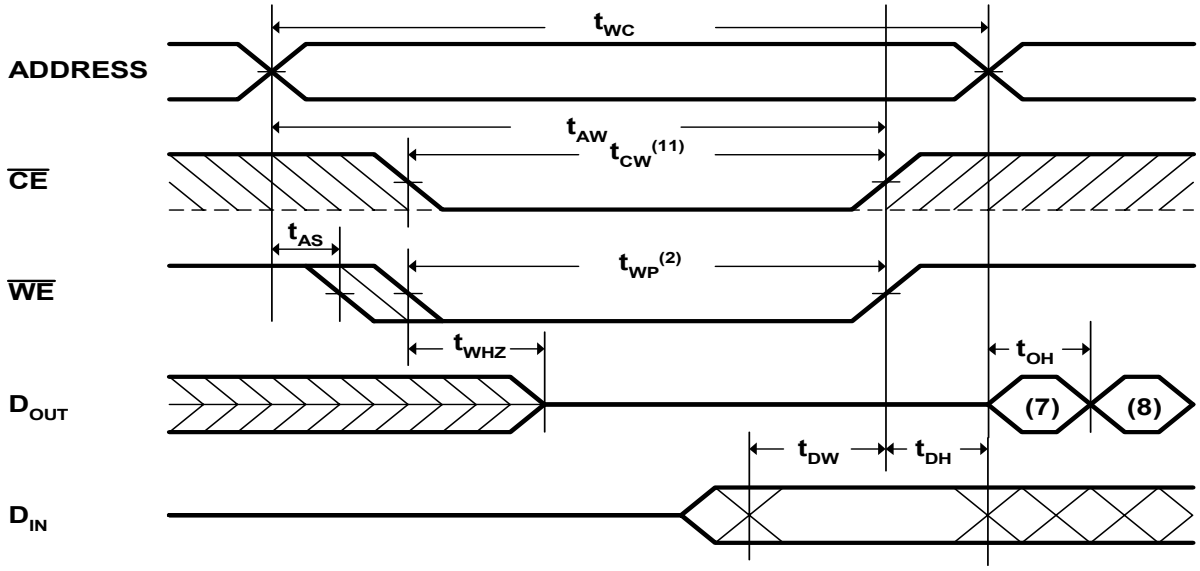
JEDEC Name	Symbol	Description	-55		-70		Unit
			MIN	MAX	MIN	MAX	
t_{AVAX}	t_{WC}	Write Cycle Time	55		70		ns
t_{E1LWH}	t_{CW}	Chip Select to End of Write	55		70		ns
t_{AVWL}	t_{AS}	Address Setup Time	0		0		ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	55		70		ns
t_{WLWH}	t_{WP}	Write Pulse Width	40		50		ns
t_{WHAX}	t_{WR}	Write Recovery Time	0		0		ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z		25		35	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap	20		30		ns
t_{WHDX}	t_{DH}	Data Hold for Write End	0		0		ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	0	30	0	30	ns
t_{WHOX}	t_{OW}	End of Write to Output Active	5		5		ns

■ SWITCHING WAVEFORMS (WRITE CYCLE)

WRITECYCLE1(1)



WRITE CYCLE2(1,6)

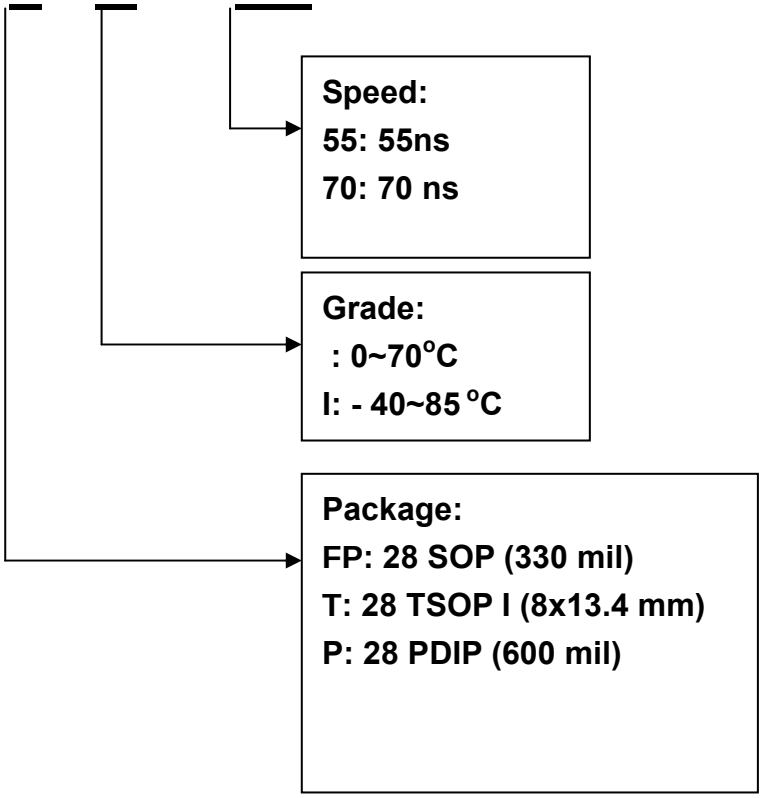


NOTES:

1. /WE must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of /CE and /WE low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. T_{WR} is measured from the earlier of /CE or /WE going high at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the /CE low transition occurs simultaneously with the /WE low transitions or after the /WE transition, output remain in a high impedance state.
6. /OE is continuously low (/OE = V_{IL}).D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If /CE is low during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ±500mV from steady state with C_L = 5pF as shown in Figure 1B. The parameter is guaranteed but not 100% tested.
11. T_{CW} is measured from the later of /CE going low to the end of write.

■ ORDER INFORMATION

WS6264LL P G – HH

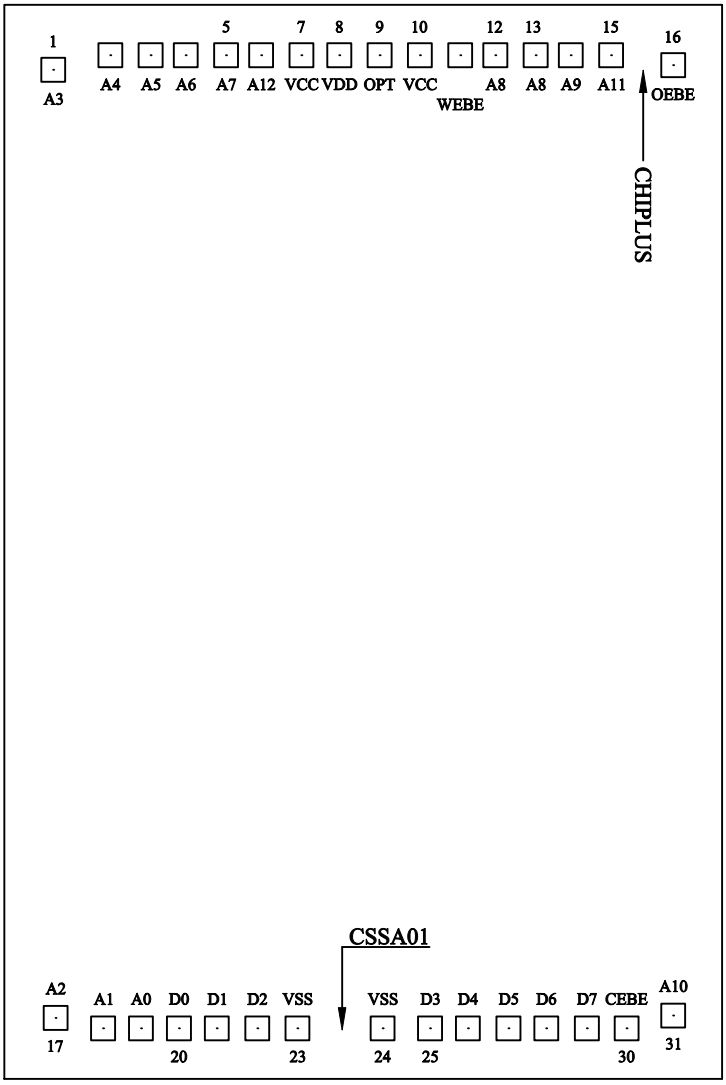


Die Information

Device: CSSA01

Date: 07/14/2004

Density: 64K Low Power SRAM (8Kx8) w/o CE2



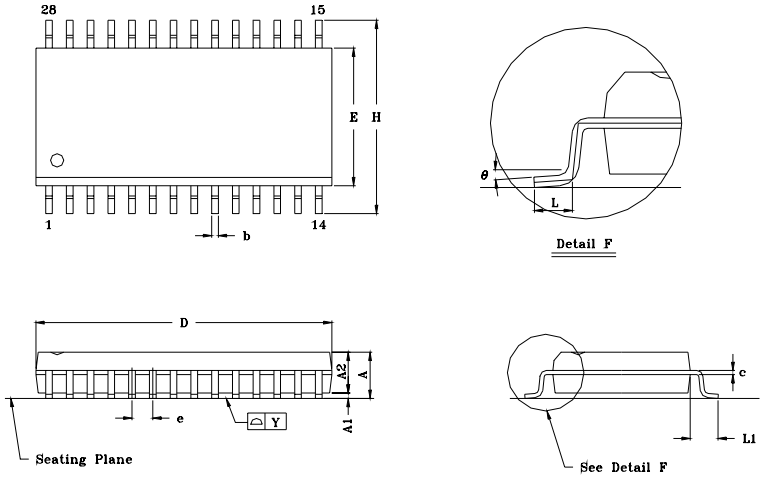
Pad no.	Pad name	Pad coordinate	
		X (um)	Y (um)
1	A3	72.00	3072.40
2	A4	249.45	3117.60
3	A5	374.65	3117.60
4	A6	483.65	3117.60
5	A7	608.85	3117.60
6	A12	717.85	3117.60
7	VCC	843.05	3117.60
8	VDD	960.65	3117.60
9	OPT	1085.85	3117.60
10	VCC	1211.05	3117.60
11	WEBE	1336.25	3117.60
12	A8	1445.25	3117.60
13	A8	1570.45	3117.60
14	A9	1679.45	3117.60
15	A11	1804.65	3117.60
16	OEBE	1997.60	3086.80
17	A2	79.50	127.80
18	A1	226.95	95.30
19	A0	344.55	95.30
20	D0	462.55	95.30
21	D1	580.05	95.30
22	D2	706.05	95.30
23	VSS	830.50	95.30
24	VSS	1095.15	95.30
25	D3	1242.50	95.30
26	D4	1360.00	95.30
27	D5	1486.00	95.30
28	D6	1603.50	95.30
29	D7	1732.50	95.30
30	CEBE	1844.95	95.30
31	A10	1997.60	135.00

Note:

1. Chip size: 2229um x 3336um (included the scribe line 80um x 80um)
2. Bond pad size: 100um x 100um
   Bond pad opening size: 90um x 90um
3. Min. bond pad pitch: 109um
4. Left down of dice: (0,0)
5. For 5V:
   Pad#8 VDD & Pad#9 OPT: Non-Connection
   Pad#7 & #10 VCC: please tie to VCC

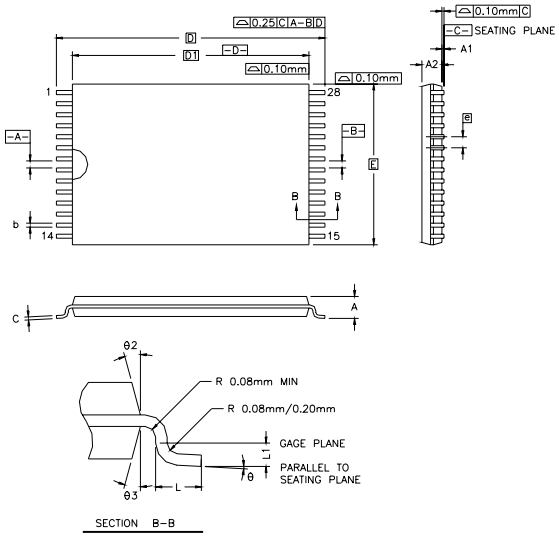
■ PACKAGE DIMENSIONS

- **28 pin SOP (330 mil) :**



SYMBOL / UNIT		A	A1	A2	b	c	D	E	e	H	L	L1	Y	θ
mm	Min.	---	0.102	2.362	0.355	0.203	---	8.280	1.118	11.506	0.711	1.499	---	0°
	Nom.	---	---	2.489	0.406	0.254	18.110	8.407	1.270	11.811	0.914	1.702	---	---
	Max.	2.845	---	2.616	0.508	0.356	18.618	8.534	1.422	12.116	1.117	1.905	0.102	10°
Inch	Min.	---	0.004	0.093	0.014	0.008	---	0.326	0.044	0.453	0.028	0.059	---	0°
	Nom.	---	---	0.098	0.016	0.010	0.713	0.331	0.050	0.465	0.036	0.067	---	---
	Max.	0.112	---	0.103	0.020	0.014	0.733	0.336	0.056	0.477	0.044	0.075	0.004	10°

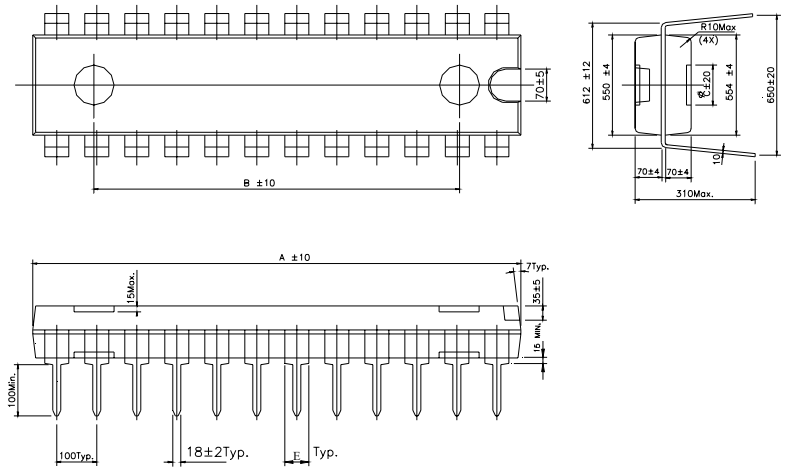
- **28 pin TSOP I (8x13.4 mm) :**



SYMBOL / UNIT		A	A1	A2	b	c	D1	E	D	e	L	L1	θ	θ2	θ3
mm	Min.	---	0.05	0.90	0.17	0.10	11.8 bsc	8.00 bsc	13.40 bsc	0.55 bsc	0.50	0.25 bsc	0°	15° REF	15° REF
	Nom.	---	---	1.00	0.20	0.15					0.60		3°		
	Max.	1.20	0.15	1.05	0.27	0.21					0.70		5°		
Inch	Min.	---	0.002	0.035	0.007	0.004	0.465 bsc	0.315 bsc	0.528 bsc	0.022 bsc	0.020	0.010 bsc	0°	15° REF	15° REF
	Nom.	---	---	0.040	0.008	0.006					0.024		3°		
	Max.	0.047	0.006	0.041	0.011	0.008					0.028		5°		

- **28 pin PDIP (600mil):**

Unit: mil



LD	A	B	C	E
28	1450	965	125	60