



**WS7107CPLG (MK)**

## 3 1/2 Digit LED Display A/D Converter

### FEATURES

- Guaranteed zero reading for 0V input on all scales
- True polarity at zero for precise null detection
- True differential input and reference, direct LED display drive
- Low noise – less than 15 $\mu$ Vp-p
- On-chip clock and a reference
- Low power dissipation – less than 10mW typically
- No additional active circuits required
- New small outline surface mount package available

### DESCRIPTION

The WS7107CPLG is a high performance, low power 3 1/2 digit A/D converter, which includes seven segment decoders, display drivers, a reference, and a clock. The WS7107CPLG is capable of directly driving an instrument size light emitting diode (LED) display.

The WS7107CPLG combines high accuracy, versatility, and true economy. True differential inputs and a reference are useful in all systems, but give a designer an uncommon advantage when measuring load cells, strain gauges and other bridge-type transducers.

### ABSOLUTE MAXIMUM RATINGS

Supply voltage

WS7107CPLG V+ to GND.....6V

WS7107CPLG V- to GND.....-9V

Analog input voltage (either input) (Note 1).... V+ to V-

Reference input voltage (either input) .....V+ to V-

Clock input

WS7107CPLG

GND to V+

### ELECTRICAL SPECIFICATIONS (Note 2)

Parameters	Test conditions	Min	Typ	Max	Unit
<b>SYSTEMS PERFORMANCE</b>					
Zero input reading	V <sub>IN</sub> = 0.0V, Full-scale = 200mV	-000.0	±000.0	±000.0	Digital reading
Ratiometric reading	V <sub>IN</sub> = V <sub>REF</sub> , V <sub>REF</sub> = 100mV	999	999/1000	1000	Digital reading
Rollover error	-V <sub>IN</sub> = +V <sub>IN</sub> ≅ 200mV Difference in the reading for equal positive and negative inputs near full-scale	-1	-	+1	Counts
Linearity	Full-scale = 200mV or Full-scale = 2V Maximum. Deviation from the best straight line fit (Note 3)	-1	-	+1	Counts
Common mode rejection ratio	V <sub>CM</sub> = 1V, V <sub>IN</sub> = 0V, Full-Scale = 200mV (Note 3)	-	50	-	$\mu$ V/V
End power supply character V+ supply current	V <sub>IN</sub> = 0 (does not include LED Current for WS7107CPLG)	-	-	1.8	mA
End power supply character V- supply current		-	-	1.8	mA
COM (Common) pin analog common voltage	25 k $\Omega$ between COM and Positive supply (with respect to + supply)	2.4	-	3.2	V
<b>DISPLAY DRIVER</b>					
Segment sinking current (Except Pins 19 and 20)	V+ = 5V, segment voltage = 3V	5	8	-	mA
Pin 19 only		10	16	-	mA
Pin 20 only		4	7	-	mA

### NOTES:

1. Input voltages may exceed the supply voltages provided the input current is limited to  $\pm 100\mu$ A
2. The Specification applies to WS7107CPLG at T<sub>A</sub> = +25°C, f<sub>CLOCK</sub> = 48 kHz. 7107M,7107MK is tested in the circuit of Figure 1.
3. Not tested, guaranteed by design.



WS7107CPLG (MK)

### 3 1/2 Digit LED Display A/D Converter

#### TYPICAL APPLICATION AND TEST CIRCUIT

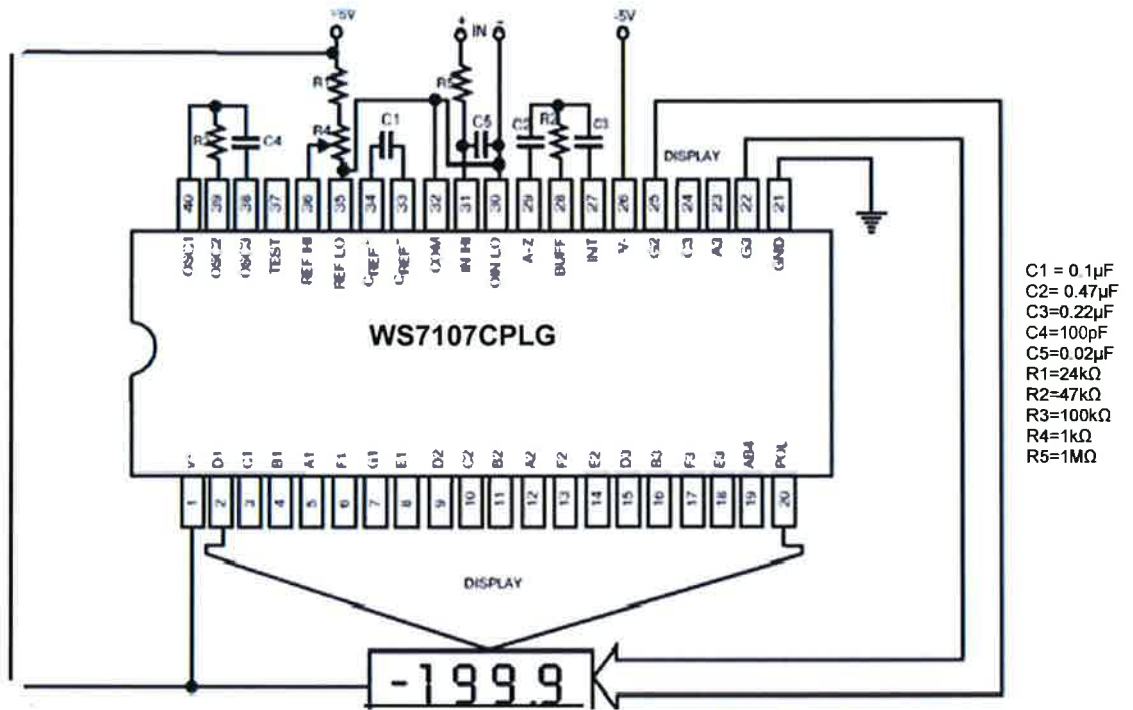
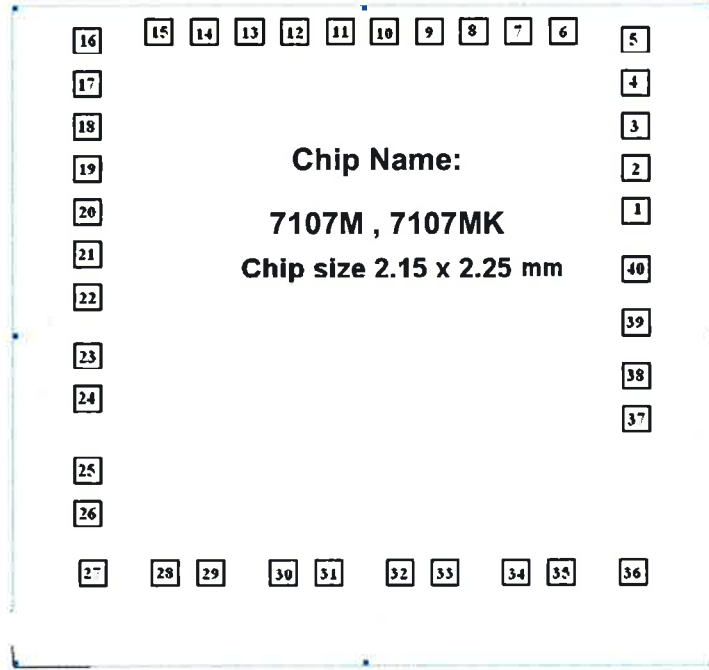


Fig.1. WS7107CPLG test circuit and typical application with LED display components selected for 200 mV full scale



**WS7107CPLG Chip Pad Location**



No.	ADC Pin	X	Y	No.	ADC Pin	X	Y
1.	V+	1990	1455	21.	GND	160	1305
2.	D1	1990	1605	22.	G3	160	1155
3.	C1	1990	1755	23.	A3	160	950
4.	B1	1990	1905	24.	C3	160	800
5.	A1	1990	2055	25.	G2	160	546
6.	F1	1750	2090	26.	V-	160	396
7.	G1	1600	2090	27.	INT	178	188
8.	E1	1450	2090	28.	BUF	418	188
9.	D2	1300	2090	29.	A/Z	568	188
10.	C2	1150	2090	30.	IN LO	808	188
11.	B2	1000	2090	31.	IN HI	958	188
12.	A2	850	2090	32.	COM	1198	188
13.	F2	700	2090	33.	C <sub>REF-</sub>	1348	188
14.	E2	550	2090	34.	C <sub>REF+</sub>	1588	188
15.	D3	400	2090	35.	REF LO	1738	188
16.	B3	160	2055	36.	REF HI	1978	188
17.	F3	160	1905	37.	TEST	1990	727
18.	E3	160	1755	38.	OSC3	1990	877
19.	AB4	160	1605	39.	OSC2	1990	1063
20.	POL	160	1455	40.	OSC1	1990	1249