



■ GENERAL DESCRIPTION

The WS628512 is a high performance, high speed, and super low power CMOS Static Random Access Memory organized as 524,288 words by 8 bits and operates from a wide range of 4.5 to 5.5V supply voltage. Advanced 0.15um CMOS technology and circuit techniques provide both high speed and low power features with a typical CMOS standby current of 0.5uA and maximum access time of 55/70ns in 5.0V operation.

The WS628512 has an automatic power down feature, reducing the power consumption significantly when chip is deselected. The WS628512 is available in JEDEC standard 32-pin sTSP 1 -8x13.4 mm, TSOP 1 -8x20mm, TSOP 2 -400mil, SOP -450 mil and PDIP -600mil packages.

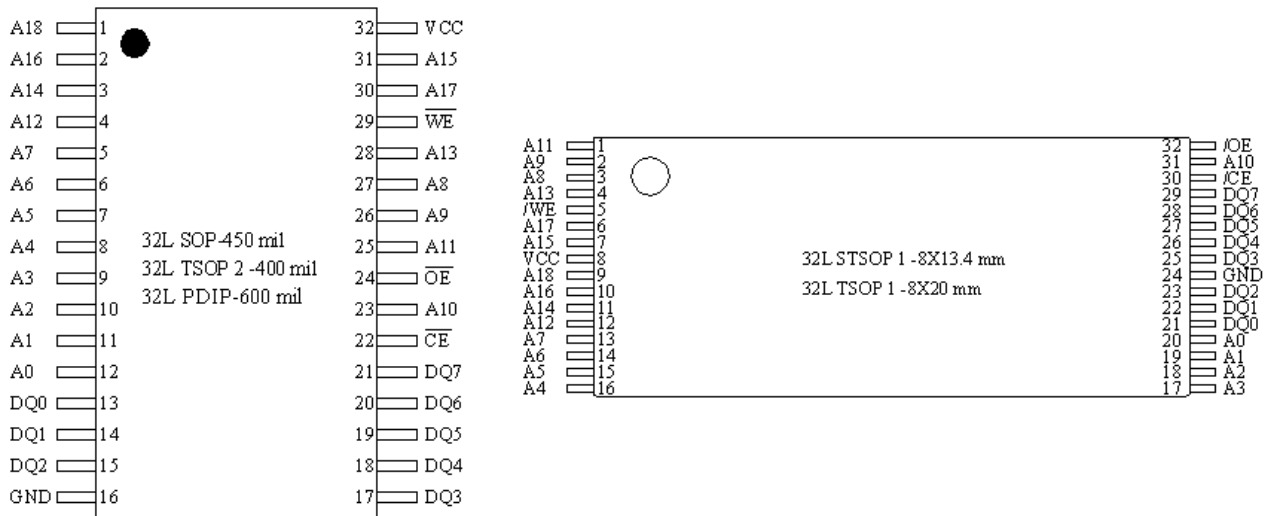
■ FEATURES

- Low operation voltage: 4.5 ~ 5.5V
Ultra low power consumption : 7mA@1MHz (Max.) operating current
0.5 uA (Typ.) CMOS standby current
- High speed access time : 55/70ns (Max.) at Vcc = 5.0V.
- Automatic power down when chip is deselected.
- Three state outputs and TTL compatible
- Data retention voltage: 1.5V(Min.)

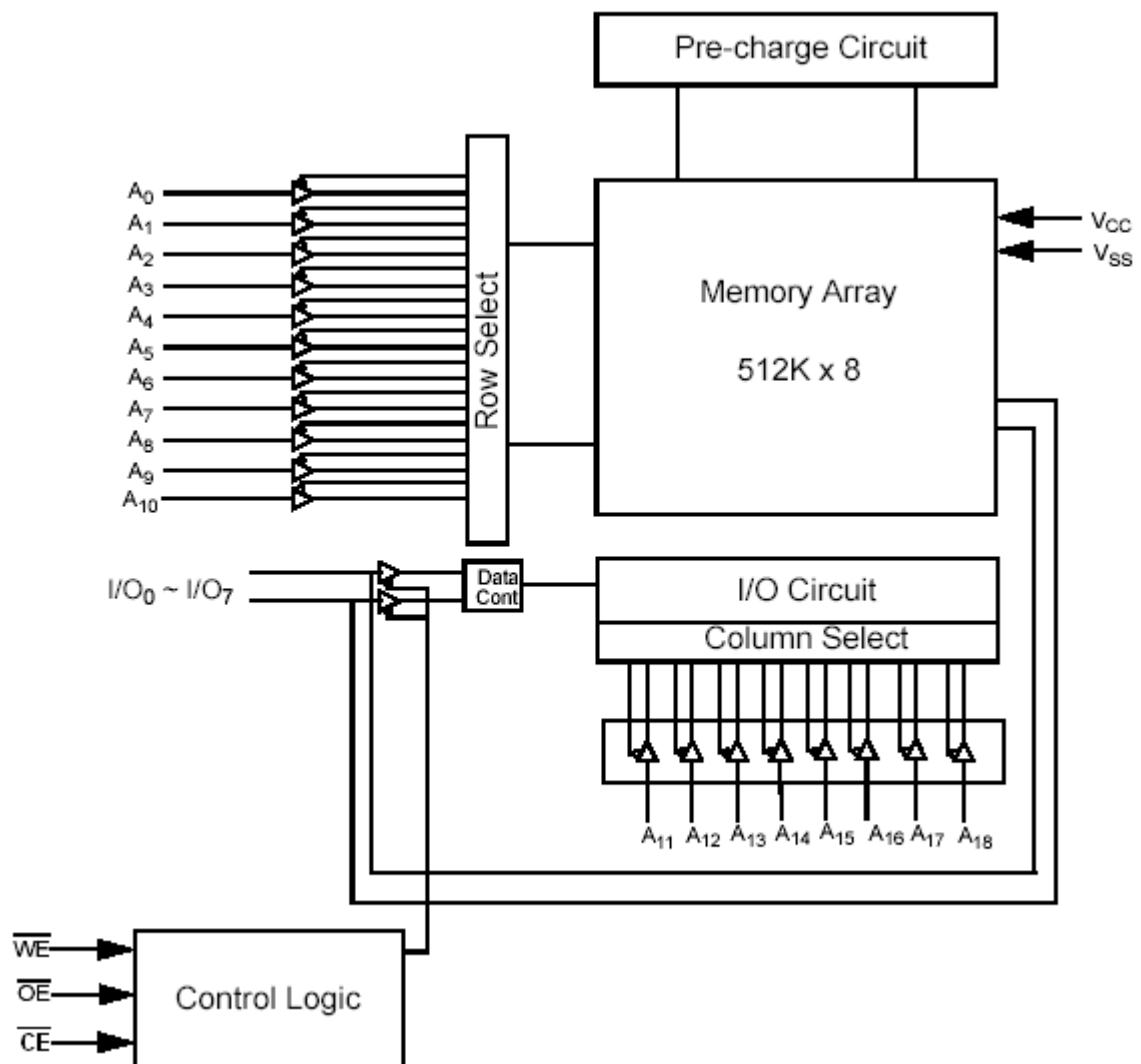
■ Product Family

Product Family	Operating Temp	Standby (Typ.) (Vcc = 5.0V)	Vcc. Range	Speed (ns)	Package Type
WS628512LLFP	0~70°C	0.5 uA	4.5~5.5	55 / 70	32L SOP
WS628512LLST					32L STSOP 1
WS628512LLT					32L TSOP 1
WS628512LLTE	32L TSOP 2				
WS628512LLP	-40~85°C	0.5 uA			32L PDIP

■ PIN CONFIGURATIONS



■ FUNCTIONAL BLOCK DIAGRAM



■ PIN DESCRIPTIONS

Name	Type	Function
A0 – A18	Input	Address inputs for selecting one of the 524,288 x 8 bit words in the RAM
/CE	Input	/CE is active LOW. Chip enables must be active when data read from or write to the device. If either chip enable is not active, the device is deselected and in a standby power down mode.
/WE	Input	The Write enable input is active LOW. It controls read and write operations. With the chip selected, when /WE is HIGH and /OE is LOW, output data will be present on the DQ pins, when /WE is LOW, the data present on the DQ pins will be written into the selected memory location.
/OE	Input	The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled.
DQ0~DQ7	I/O	These 8 bi-directional ports are used to read data from or write data into the RAM.
V _{CC}	Power	Power Supply
V _{SS}	Power	Ground
NC		No connection

■ TRUTH TABLE

MODE	/CE	/WE	/OE	DQ0~7	V _{CC} Current
Standby	H	X	X	High Z	I _{CCSB} , I _{CCSB1}
Output Disabled	L	H	H	High Z	I _{CC}
Read	L	H	L	D _{OUT}	I _{CC}
Write	L	L	X	D _{IN}	I _{CC}

Note: X means don't care. (Must be low or high state)

■ ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Rating	Unit
V _{IN} , V _{OUT}	Voltage on any pin relative to V _{SS}	-0.5 to 6.0	V
V _{CC}	Voltage on V _{CC} supply relative to V _{SS}	-0.5 to 6.0	V
P _D	Power Dissipation	1.0	W

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

■ OPERATING RANGE

Range	Ambient Temperature	Vcc
Commercial	0~70°C	4.5V ~ 5.5V
Industrial	-40~85°C	4.5V ~ 5.5V

1. Overshoot : Vcc +1.0V in case of pulse width ≤ 20 ns.
2. Undershoot : - 1.0V in case of pulse width ≤ 20 ns.
3. Overshoot and undershoot are sampled, not 100% tested.

■ CAPACITANCE ⁽¹⁾ (T_A = 25°C, f = 1.0 MHz)

Symbol	Parameter	Conditions	MAX.	Unit
C _{IN}	Input Capacitance	V _{IN} =0V	8	pF
C _{DO}	Input/Output Capacitance	V _{IO} =0V	10	pF

1. This parameter is guaranteed and not tested.

■ DC ELECTRICAL CHARACTERISTICS (T_A = 0 to + 70°C , Vcc = 5.0V)

Parameter Name	Parameter	Test Conduction	MIN	TYP ⁽¹⁾	MAX	Unit
V _{IL}	Guaranteed Input Low Voltage ⁽²⁾		-0.5		0.6	V
V _{IH}	Guaranteed Input High Voltage ⁽²⁾		2.2		Vcc+0.5	V
I _{IL}	Input Leakage Current	V _{CC} =MAX, V _{IN} =0 to V _{CC}	-1		1	uA
I _{OL}	Output Leakage Current	V _{CC} =MAX, /CE=V _{IH} , or /OE=V _{IH} , or /WE= V _{IL} , V _{IO} =0V to V _{CC}	-1		1	uA
V _{OL}	Output Low Voltage	V _{CC} =MAX, I _{OL} = 2.1mA			0.4	V
V _{OH}	Output High Voltage	V _{CC} =MIN, I _{OH} = -1.0mA	2.4			V
I _{CC}	Operating Power Supply Current	/CE=V _{IL} , I _{IO} =0mA, F=F _{MAX} ⁽³⁾ , 100%duty, V _{IN} = V _{IL} or V _{IH}	55		55	mA
			70		45	
I _{CCSB}	Standby Supply - TTL	/CE=V _{IH} , I _{UO} =0mA, other pins= V _{IL} or V _{IH}			1	mA
I _{CCSB1}	Standby Current -CMOS	/CE \geq V _{CC} -0.2V, V _{IN} \geq V _{CC} -0.2V or V _{IN} \leq 0.2V		0.5	20	uA

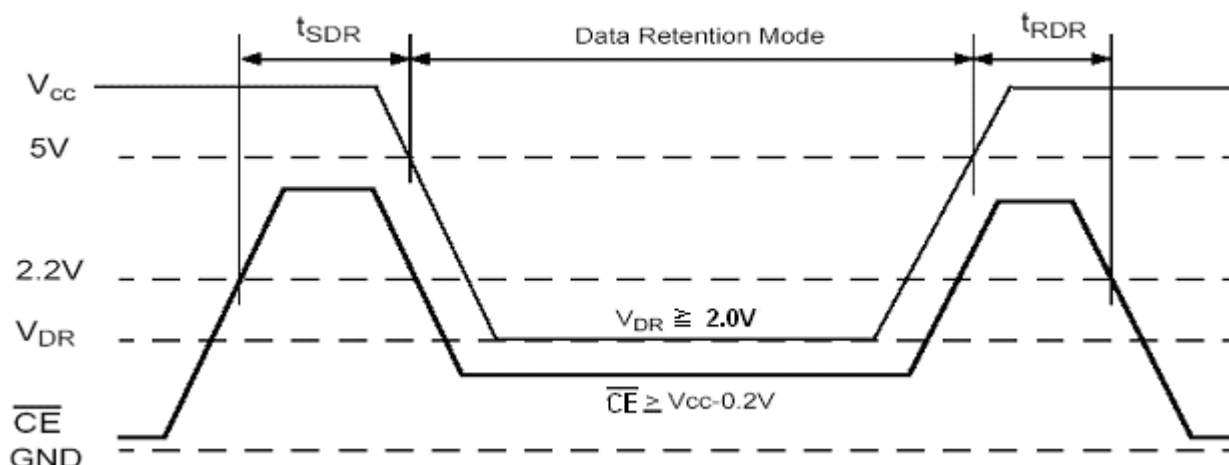
1. Typical characteristics are at T_A = 25°C and not 100% tested.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. Fmax = 1/t_{RC}.

■ DATA RETENTION CHARACTERISTICS ($T_A = 0$ to $+70^\circ\text{C}$)

Parameter Name	Parameter	Test Conduction	MIN	TYP	MAX	Unit
V_{DR}	V_{CC} for Data Retention	$\overline{CE} \geq V_{CC}-0.2V$, $V_{IN} \geq V_{CC}-0.2V$ or $V_{IN} \leq 0.2V$	2.0			V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{CC}-0.2V$, $V_{CC}=2.0V$ $V_{IN} \geq V_{CC}-0.2V$ or $V_{IN} \leq 0.2V$		0.5	7	μA
t_{SDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0			ns
t_{RDR}	Operation Recovery Time		t_{RC} (1)			ns

1.Read Cycle Time

■ LOW V_{CC} DATA RETENTION WAVEFORM (\overline{CE} Controlled)



■ AC TEST CONDITIONS

Input Pulse Levels: $V_{CC}/0V$

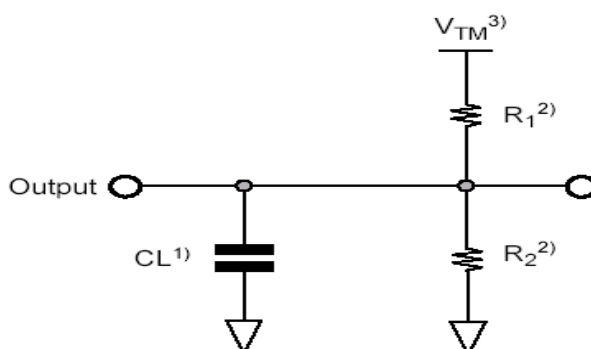
Input Rise and Fall Times: 1V/ns

Input and Output Timing Reference Level: 0.5 V_{CC}

Output Load (See right)

$CL^{(1)}$: 100pF + 1TTL(70ns)

$CL^{(1)}$: 30pF + 1 TTL(55ns)



Note: 1. Including scope and jig capacitance

2. $R_1=1800$ ohm, $R_2=990$ ohm

3. $V_{TM} = V_{CC}$

4. $L = 5pF + 1$ TTL (measurement with t_{LZ} , t_{OLZ} , t_{OHZ} , t_{WHZ})

KEY TO SWITCHING WAVEFORMS

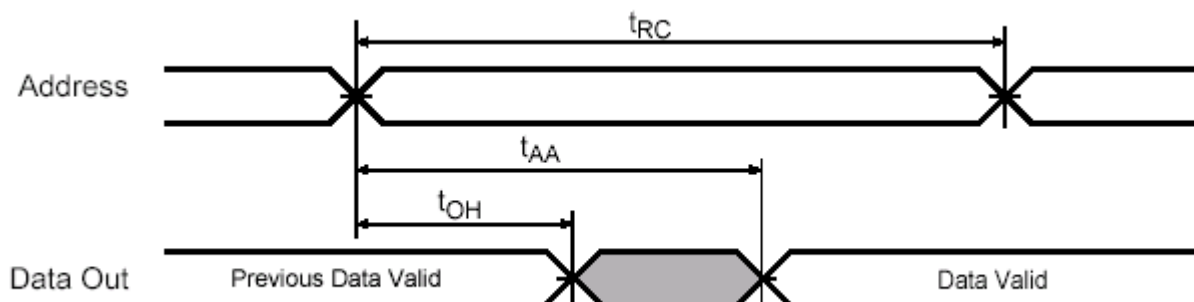
WAVEFORMS	INPUTS	OUTPUTS
	MUST BE STEADY	MUST BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGE FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGE STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE OFF STATE

AC ELECTRICAL CHARACTERISTICS ($T_A = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5.0\text{V}$)
[READ CYCLE]

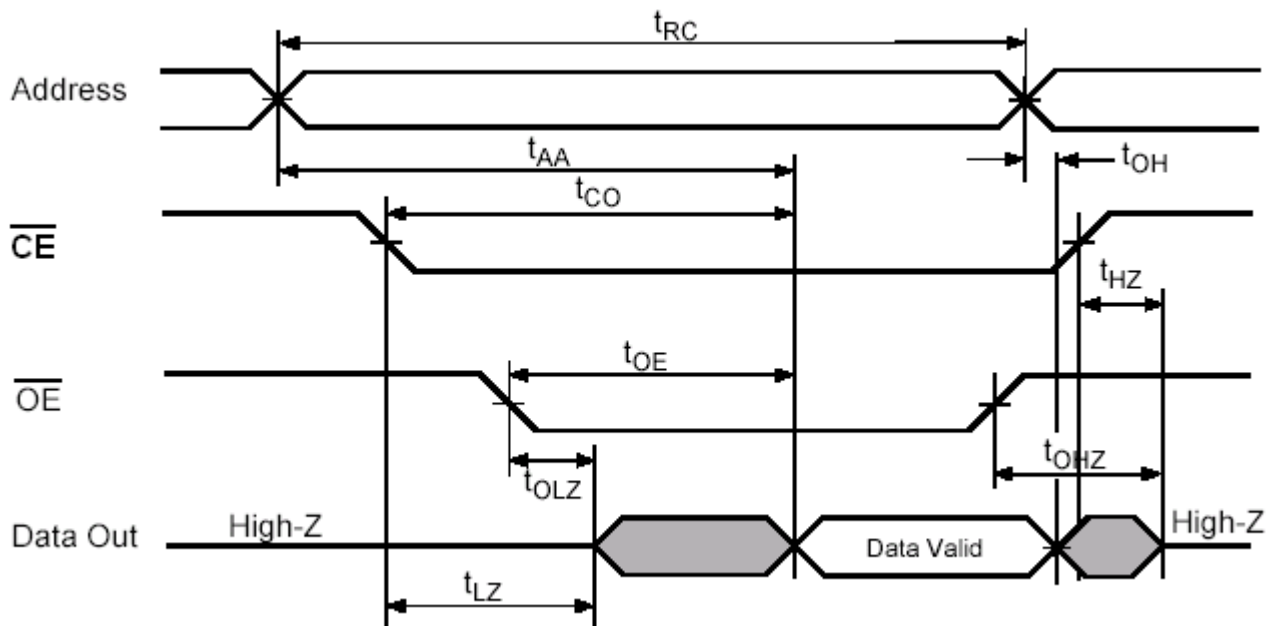
JEDEC Name	Parameter Name	Description	55		70		Unit
			MIN	MAX	MIN	MAX	
t_{AVAX}	t_{RC}	Read Cycle Time	55		70		ns
t_{AVQV}	t_{AA}	Address Access Time		55		70	ns
t_{ELQV}	t_{CO}	Chip Select Access Time (/CE)		55		70	ns
t_{GLQV}	t_{OE}	Output Enable to Output Valid		30		35	ns
t_{ELQX}	t_{LZ}	Chip Select to Output Low Z (/CE)	10		10		ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	5		5		ns
t_{EHQZ}	t_{HZ}	Chip Deselect to Output in High Z (/CE)	0	20	0	25	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	0	20	0	25	ns
t_{AXOX}	t_{OH}	Out Disable to Address Change	10		10		ns

SWITCHING WAVEFORMS

READ CYCLE (1) (Address Transition Controlled)



READ CYCLE (2) (/OE Controlled)



NOTES:

1. t_{HZ} and t_{OHZ} are defined as the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.

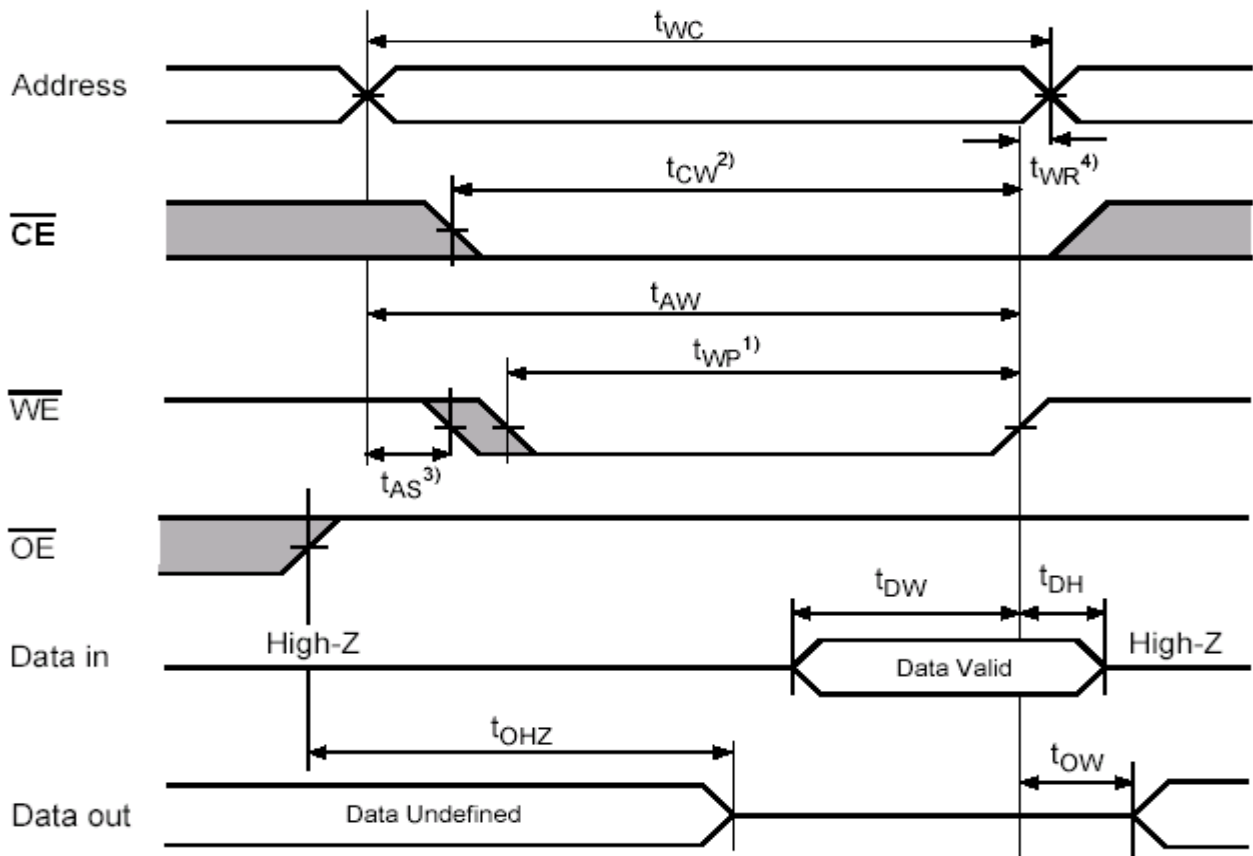
■ AC ELECTRICAL CHARACTERISTICS ($T_A = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5.0\text{V}$)

[WRITE CYCLE]

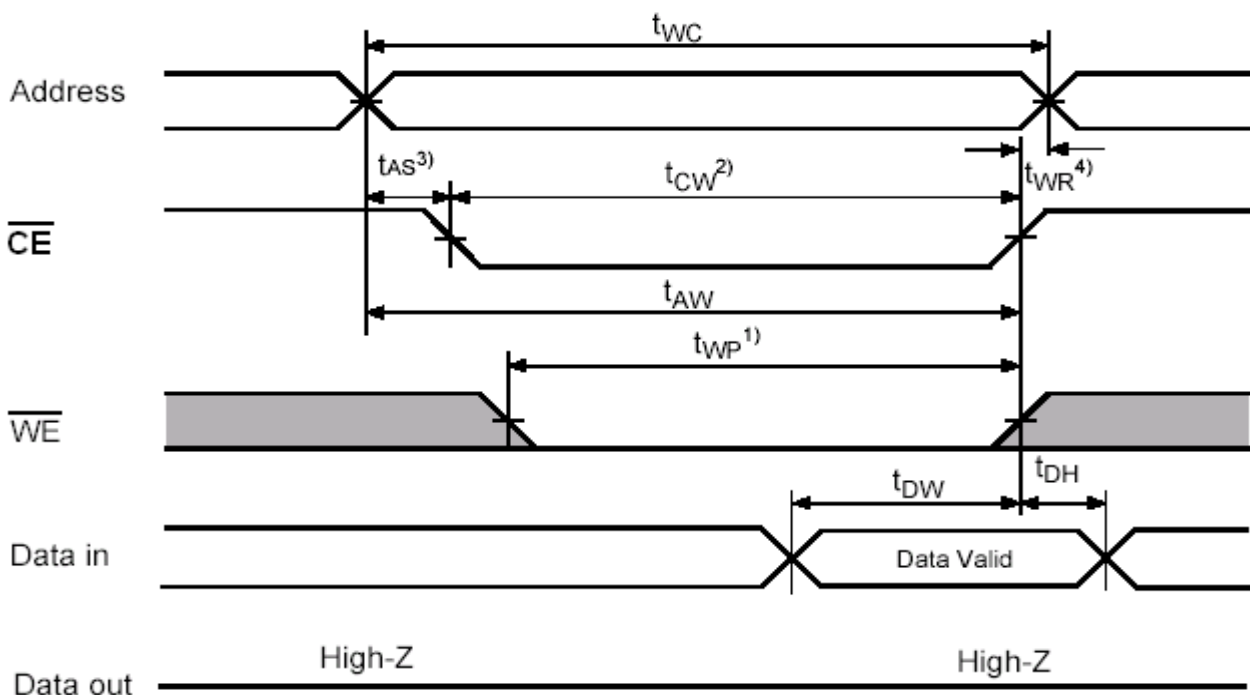
JEDEC Name	Parameter Name	Description	55		70		Unit
			MIN	MAX	MIN	MAX	
t_{AVAX}	t_{WC}	Write Cycle Time	55		70		ns
t_{E1LWH}	t_{CW}	Chip Select to End of Write	45		60		ns
t_{AVWL}	t_{AS}	Address Setup Time	0		0		ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	45		60		ns
t_{WLWH}	t_{WP}	Write Pulse Width	40		50		ns
t_{WHAX}	t_{WR}	Write Recovery Time (/CE, /WE)	0		0		ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z	0	20	0	20	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap	25		30		ns
t_{WHDX}	t_{DH}	Data Hold from Write Time	0		0		ns
t_{WHOX}	t_{OW}	End of Write to Output Active	5		5		ns

■ SWITCHING WAVEFORMS

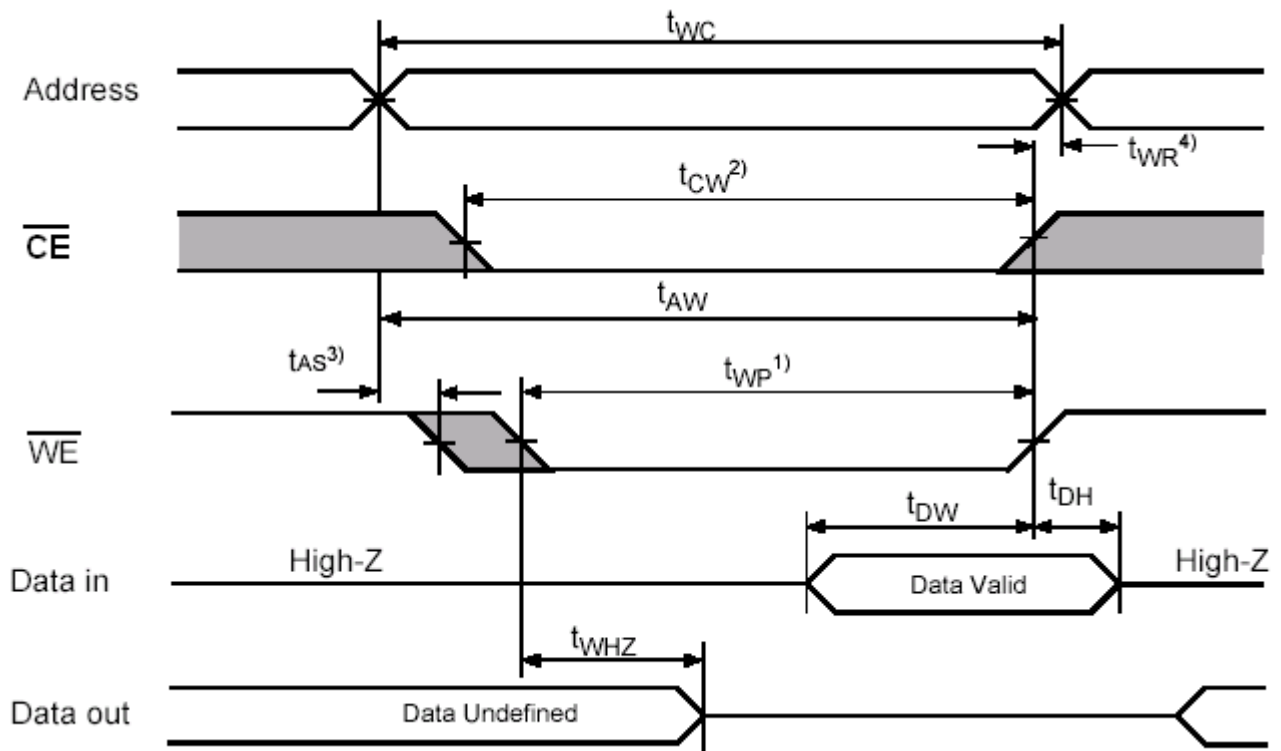
WRITE CYCLE (1) (/WE Controlled, /OE High During WRITE)



WRITE CYCLE (2) (/CE Controlled)



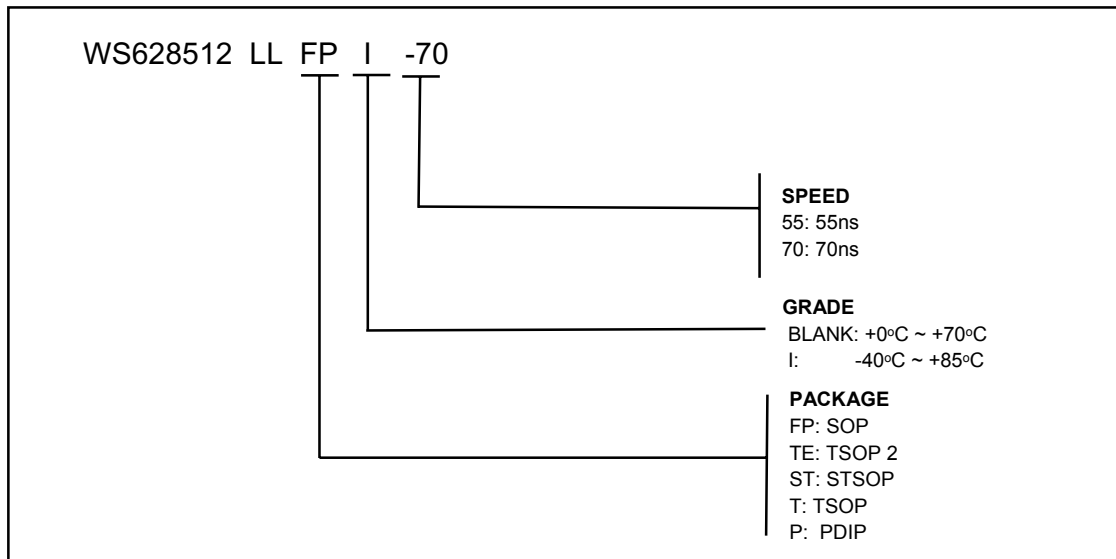
WRITE CYCLE (3) (/WE Controlled, /OE LOW)



NOTES:

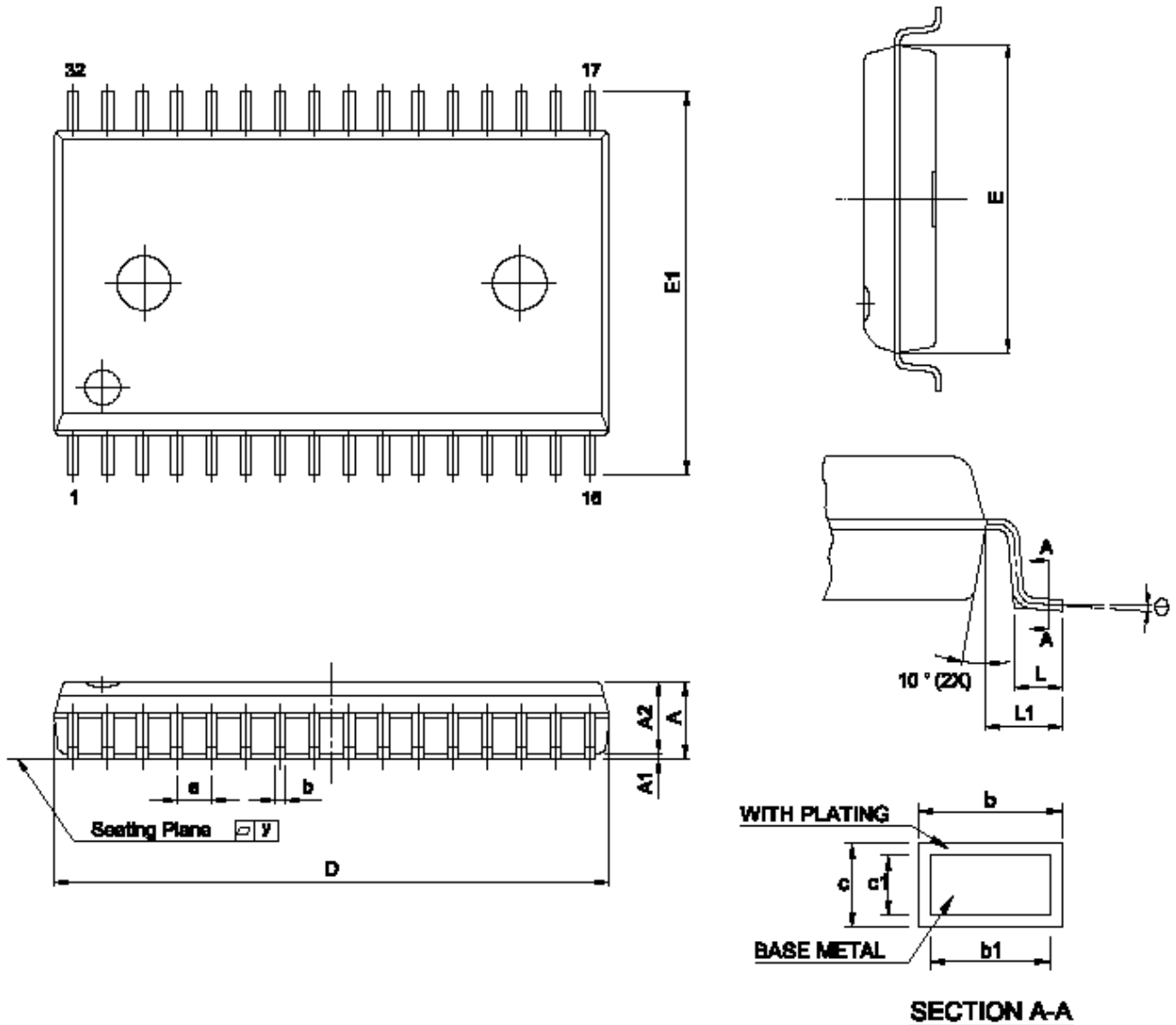
1. A write occurs during the overlap($t_{WP}^{1)}$) of low /CE and low /WE. A write begins at the latest transition among /CE goes low and /WE goes low. A write ends at the earliest transition when /CE goes high and /WE goes high. The $t_{WP}^{1)}$ is measured from the beginning of write to the end of write.
2. $t_{CW}^{2)}$ is measured from the /CE going low to end of write.
3. $t_{AS}^{3)}$ is measured from the address valid to the beginning of write.
4. $t_{WR}^{4)}$ is measured from the end of write to the address change. $t_{WR}^{4)}$ applied in case a write ends as /CE or /WE going high.

■ ORDER INFORMATION



Note: Package material code "G" meets ROHS

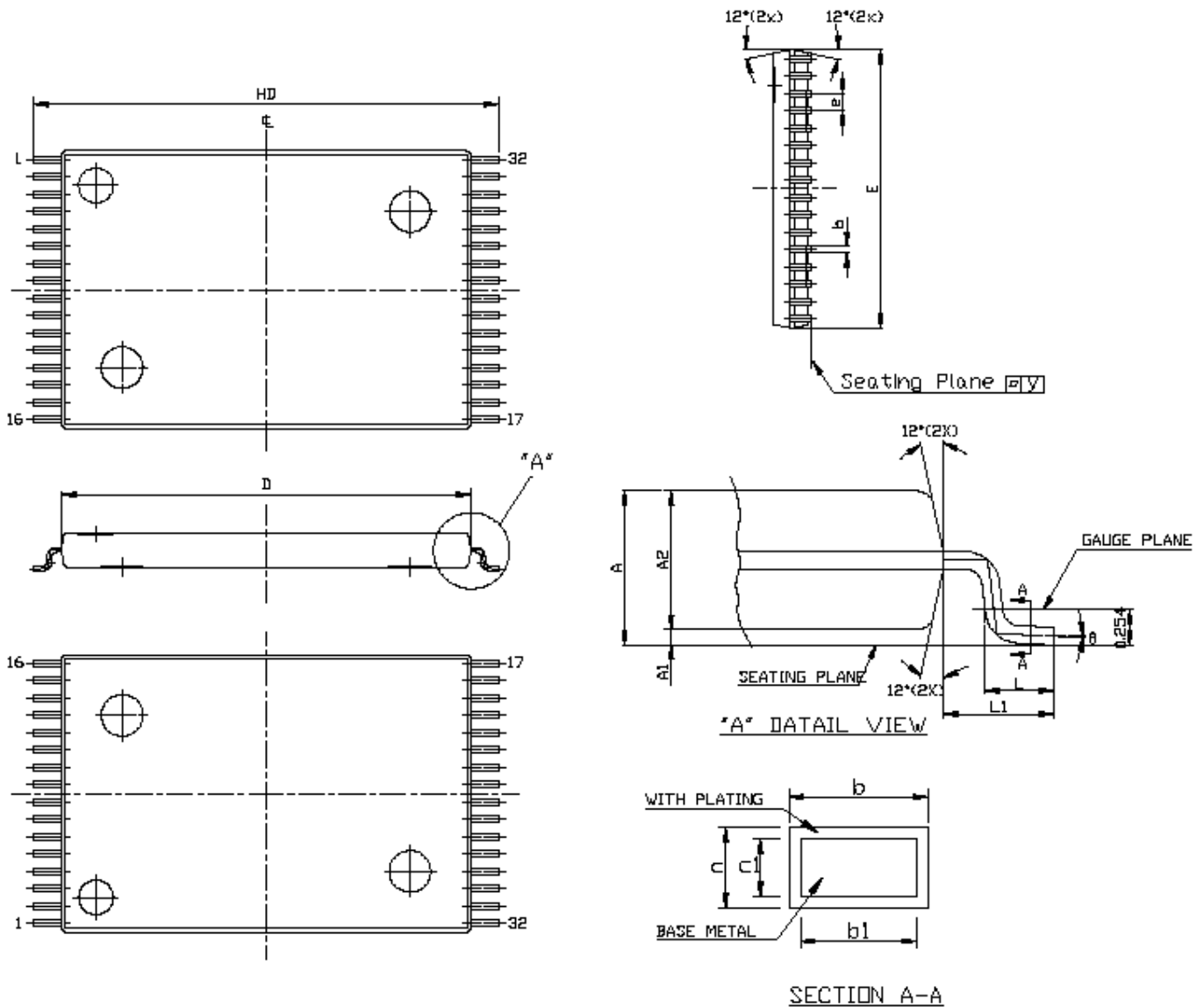
■ PACKAGE DIMENSIONS - 32L SOP 450 mll



SECTION A-A

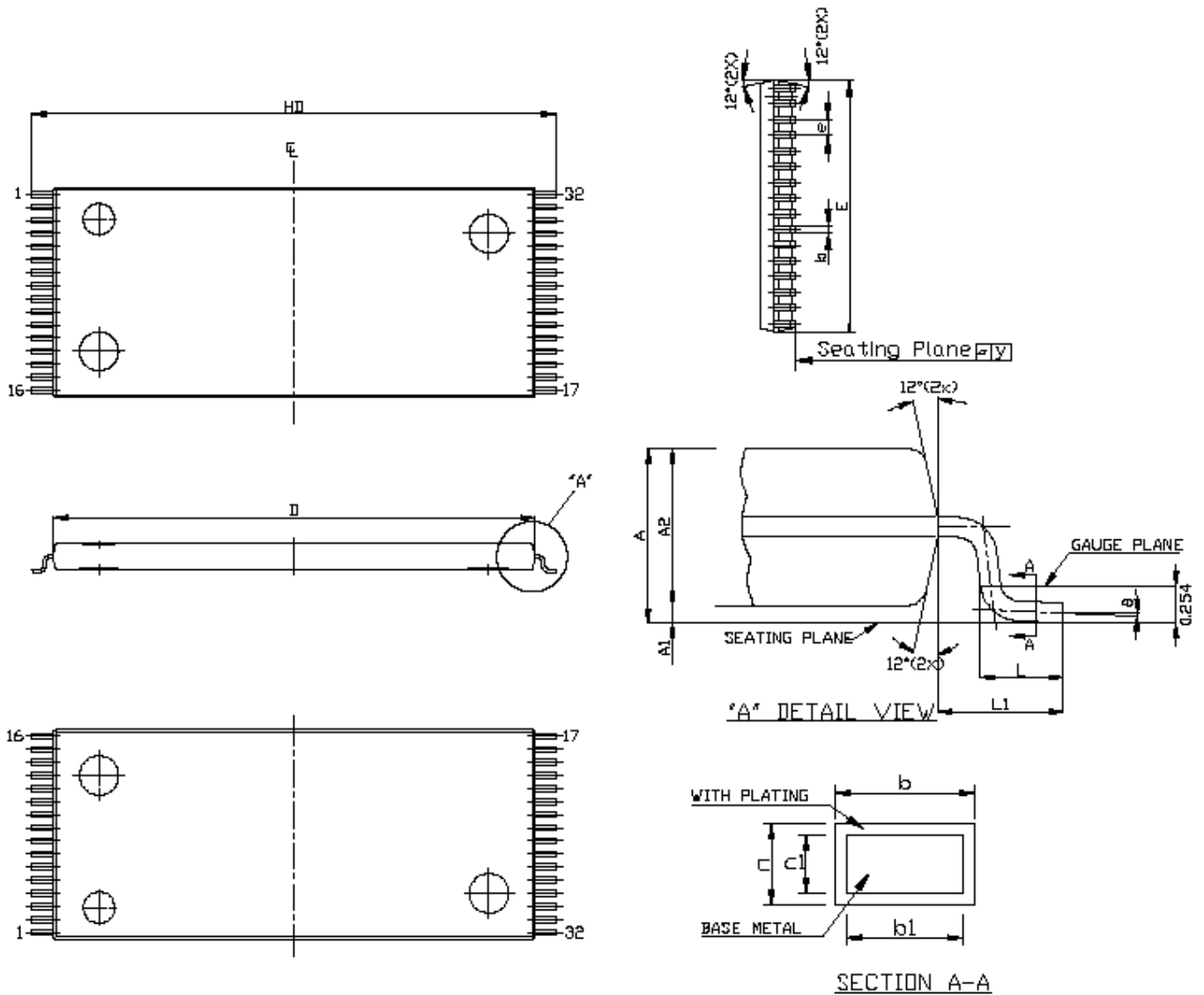
SYMBOL		A	A1	A2	b	b1	c	c1	D	E	E1	e	L	L1	y	θ
UNIT																
mm	Min.	2.645	0.102	2.540	0.35	0.35	0.15	0.15	20.320	11.178	13.792	1.118	0.584	1.194	-	0°
	Nom.	2.821	0.229	2.680	-	-	-	-	20.447	11.303	14.097	1.270	0.834	1.397	-	-
	Max.	2.997	0.358	2.820	0.50	0.48	0.32	0.28	20.574	11.430	14.402	1.422	1.084	1.800	0.1	10°
Inch	Min.	0.104	0.004	0.1000	0.014	0.014	0.006	0.006	0.800	0.440	0.543	0.044	0.023	0.047	-	0°
	Nom.	0.111	0.009	0.1055	-	-	-	-	0.805	0.445	0.555	0.050	0.033	0.055	-	-
	Max.	0.118	0.014	0.1110	0.020	0.018	0.012	0.011	0.810	0.450	0.567	0.056	0.043	0.063	0.004	10°

■ PACKAGE DIMENSIONS: 32L STSOP 1-8x13.4mm



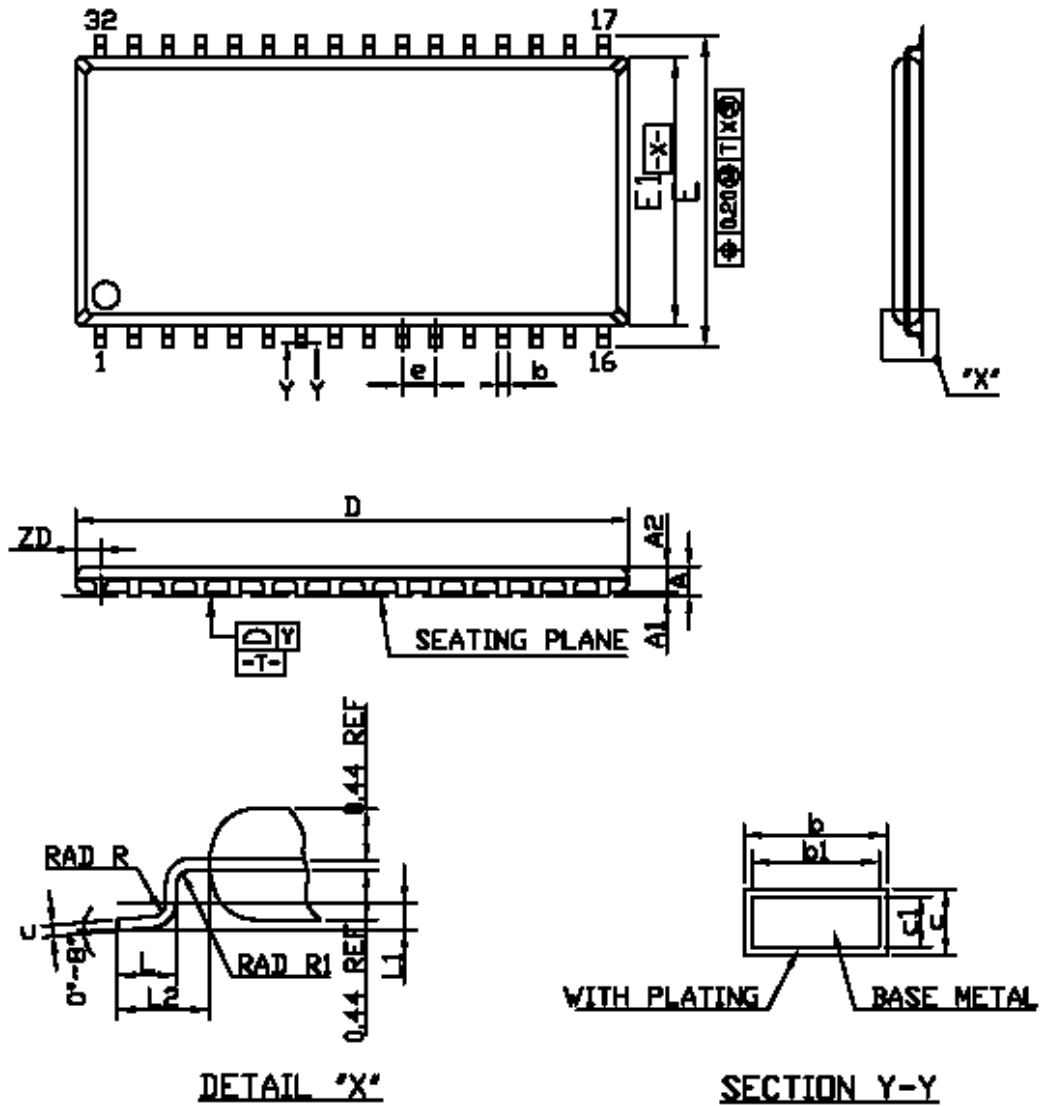
SYMBOL UNIT		A	A1	A2	b	b1	c	c1	D	E	e	HD	L	L1	y	θ
mm	Min.	1.00	0.05	0.95	0.17	0.17	0.10	0.10	11.70	7.90	0.40	13.20	0.40	0.70	-	0°
	Nom.	1.10	0.10	1.00	0.22	0.20	-	-	11.80	8.00	0.50	13.40	0.50	0.80	-	-
	Max.	1.20	0.15	1.05	0.27	0.23	0.21	0.16	11.90	8.10	0.60	13.60	0.70	0.90	0.1	8°
inch	Min.	0.0393	0.002	0.037	0.007	0.007	0.004	0.004	0.461	0.311	0.016	0.520	0.0157	0.0275	-	0°
	Nom.	0.0433	0.004	0.039	0.009	0.008	-	-	0.465	0.315	0.020	0.528	0.0197	0.0315	-	-
	Max.	0.0473	0.006	0.041	0.011	0.009	0.008	0.006	0.469	0.319	0.024	0.536	0.0277	0.0355	0.004	8°

■ PACKAGE DIMENSIONS: 32L TSOP 1-8x20mm



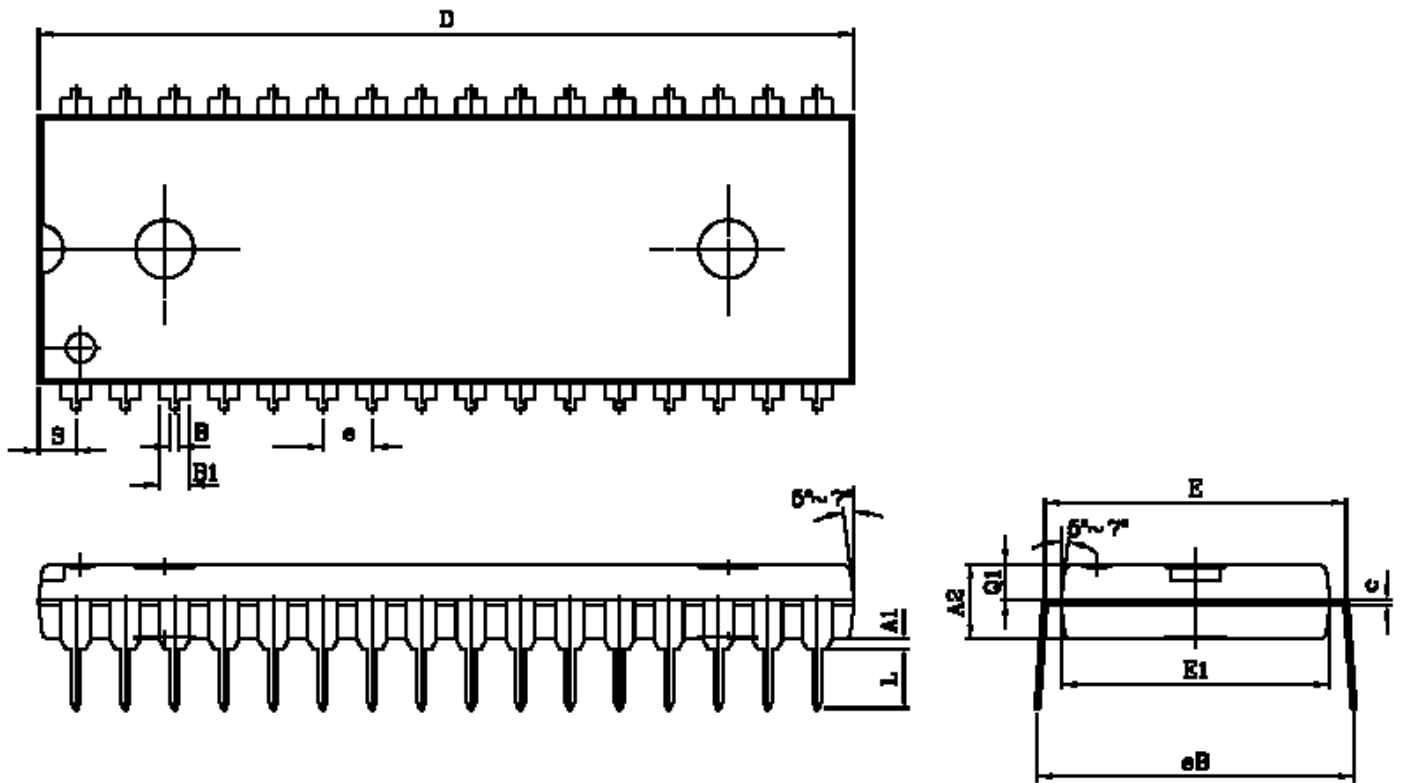
SYMBOL	A	A1	A2	b	b1	c	c1	D	E	e	HD	L	L1	y	θ	
mm	Min.	1.00	0.05	0.95	0.17	0.17	0.10	0.10	18.30	7.90	0.40	19.80	0.40	0.70	-	0°
	Nom.	1.10	0.10	1.00	0.22	0.20	-	-	18.40	8.00	0.50	20.00	0.50	0.80	-	-
	Max.	1.20	0.15	1.05	0.27	0.23	0.21	0.16	18.50	8.10	0.60	20.20	0.70	0.90	0.1	8°
inch	Min.	0.0393	0.002	0.037	0.007	0.007	0.004	0.004	0.720	0.311	0.016	0.779	0.0157	0.0275	-	0°
	Nom.	0.0433	0.004	0.039	0.009	0.008	-	-	0.724	0.315	0.020	0.787	0.0197	0.0315	-	-
	Max.	0.0473	0.006	0.041	0.011	0.009	0.008	0.006	0.728	0.319	0.024	0.795	0.0277	0.0355	0.004	8°

■ PACKAGE DIMENSIONS: 32L TSOP 2-400mil



SYMBOL	A	A1	A2	b	b1	c	c1	D	E	E1	e	L	L1	L2	R	R1	ZD	Y			
mm	Min.	-	0.05	0.95	0.30	0.30	0.12	0.10	20.82	11.56	10.03	1.27 bsc	0.40	0.25 bsc	0.8 ref	0.12	0.12	0.95 ref	-		
	Nom.	-	0.10	1.00	-	0.40	-	0.127	20.95	11.76	10.16		0.50			-	-		0.25	-	0.10
	Max.	1.20	0.15	1.05	0.52	0.45	0.21	0.16	21.08	11.96	10.29		0.60			0.010	0.031		0.005	0.005	0.037
Inch	Min.	-	0.002	0.037	0.012	0.012	0.005	0.004	0.820	0.455	0.394	0.050 bsc	0.016	0.010 bsc	0.031 ref	0.005	0.005	0.037 ref	-		
	Nom.	-	0.004	0.039	-	0.016	-	0.005	0.825	0.463	0.400		0.020			-	-		0.010	-	0.004
	Max.	0.047	0.006	0.042	0.020	0.018	0.008	0.006	0.830	0.471	0.405		0.024			0.010	-		-	-	0.004

■ PACKAGE DIMENSIONS - 32L PDIP -600mil



SYMBOL		A1	A2	B	B1	c	D	E	E1	e	eB	L	S	Q1
UNIT														
mm	Min.	0.254	3.785	0.330	1.143	0.152	41.783	14.988	13.718	2.540 (TYP)	16.002	3.048	1.851	1.851
	Norm.	-	3.912	0.457	1.270	0.254	41.910	15.240	13.818		16.510	3.302	1.905	1.778
	Max.	-	4.039	0.584	1.397	0.356	42.037	15.494	13.920		17.018	3.556	2.159	1.905
inch	Min.	0.010	0.149	0.013	0.045	0.006	1.645	0.590	0.540	0.100 (TYP)	0.630	0.120	0.065	0.065
	Norm.	-	0.154	0.018	0.050	0.010	1.650	0.600	0.544		0.850	0.130	0.075	0.070
	Max.	-	0.159	0.023	0.055	0.014	1.655	0.610	0.548		0.670	0.140	0.085	0.075